UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/672,368 | 09/28/2000 | Francis X. McKeen | 042390.P9575 | 7652 |

7590 07/23/2009

Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025

| EXAMINER | |
|---|---|
| LANIER, BENJAMIN E | |
| ART UNIT | PAPER NUMBER |
| 2432 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 07/23/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

---

*Ex parte* FRANCIS X. MCKEEN, LAWRENCE O. SMITH, BENJAMIN CRAWFORD CHAFFIN, MICHAEL P. CORNABY, and BRYANT BIGBEE

---

Appeal 2008-003080
Application 09/672,368
Technology Center 2400

---

Decided:[1] July 23, 2009

---

*Before* JOSEPH L. DIXON, HOWARD B. BLANKENSHIP, and JAMES R. HUGHES, *Administrative Patent Judges*.

HUGHES, *Administrative Patent Judge*.

DECISION ON APPEAL

---

[1] The two month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

## STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-15. We have jurisdiction under 35 U.S.C. § 6(b) (2002).

We AFFIRM.

### *Appellants' Invention*

Appellants invented a platform security apparatus and method for handling asynchronous events in a secure manner utilizing multimode (normal mode and isolated mode) operation. One embodiment of the invention is a platform security method that a maintains a normal execution mode page table map and an isolated execution mode page table map, dynamically swaps between the page table maps in response to a change in execution mode, and restricts access to an isolated memory area to only bus cycle transactions performed in the isolated execution mode. (Spec. 1, ll. 3-15; 3, ll. 6-14.)[2]

[2] We refer to Appellants': Specification ("Spec.") and Appeal Brief ("App. Br.") dated January 10, 2007. We also refer to the Examiner's Answer ("Ans.") mailed July 6, 2007.

*Claims*

Independent claims 1, 9, and 12 further illustrate the invention. They read as follows:

1. A method comprising:

maintaining a first page table map for use in an isolated execution mode and a second page table map for use in a normal execution mode;

restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode;

dynamically swapping between the first page table map and the second page table map responsive to a change in execution mode;

identifying if an event is one of a class of events to be handled in the isolated execution mode;

asserting a selection signal to select the first page table map if the event is identified as one of the class of events to be handled in the isolated execution mode; and

handling the event using a table map selected by the selection signal.

9. An apparatus comprising:

a first storage location storing control data for a first page table map;

a second storage location storing control data for a second page table map;

a selection unit to select which page table map is applied responsive to receipt of an event; and

an isolated execution circuit to generate isolated access bus cycles,

wherein isolated access bus cycles are to be used if the apparatus operates in an isolated execution mode.

12. A platform comprising:

a processor executing in one of normal execution mode and isolated execution mode;

a first set of control registers to define a current memory map of the platform;

a mapping unit to dynamically load the first set of control registers responsive to an event if the event should be handled using an alternate memory map; and

an isolated execution circuit to generate isolated access bus cycles if the processor is executing in the isolated execution mode.

*References*

The Examiner relies on the following references as evidence of unpatentability:

| | | |
|---|---|---|
| Takahashi | US 5,615,263 | Mar. 25, 1997 |
| Poisner | US 5,729,760 | Mar. 17, 1998 |
| Summers | US 6,098,133 | Aug. 01, 2000 |

George Coulouris, Jean Dollimore, & Tim Kindberg, *Distributed Systems Concepts and Design, Second Ed.*, pp. 165-194 and 300-308 (Addison-Wesley 1994) (hereinafter "Coulouris").

Abraham Silberschatz & Peter Baer Galvin, *Operating System Concepts, Fifth Ed.*, pp. 94, 264, 267, 270-272, 289, 293, 402-405, and 444-445 (John Wiley & Sons 1999) (hereinafter "Silberschatz").

*Rejections*

The Examiner rejects claims 1-8 under 35 U.S.C. § 103(a) as being unpatentable over Coulouris, Silberschatz, and Summers.

The Examiner rejects claims 9-15 under 35 U.S.C. § 103(a) as being unpatentable over Takahashi and Summers.

The Examiner alternately rejects claims 9-15 under 35 U.S.C. § 103(a) as being unpatentable over Poisner and Summers.

ISSUES

*Issue 1 – Rejection of Claims 1-8 Under 35 U.S.C. § 103(a)*

*Appellants' Contentions*

Appellants contend that the Examiner improperly rejected the claims. Specifically, Appellants contend that the Examiner failed to establish a proper prima facie case of obviousness for the claims in that the Coulouris, Silberschatz, and Summers references do not teach restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode, and that Coulouris and Silberschatz are not properly combinable with Summers because the teachings of Coulouris, Silberschatz, and Summers are inconsistent and not compatible. (App. Br. 5-7.)

*Examiner's Findings and Conclusions*

The Examiner found that Coulouris, Silberschatz, and Summers teach each feature of Appellants' invention as claimed in independent claim 1 and dependent claims 2-8. (Ans. 3-10.) The Examiner found that Coulouris teaches: (1) a secure process, where threads within a process have their own software interrupt handling mechanisms, i.e., an isolated execution mode; (2) identifying an event to be handled in isolation execution mode; and (3) handling the event using a first page table map, where the first page table map is a virtual memory map. (Ans. 3-4.) The Examiner found that Silberschatz teaches: (1) maintaining a page table map for use in normal execution mode, i.e., where pages are shared between processes; (2) maintaining a page table map for use in isolated execution mode, i.e., where a process executes its own code in an isolated manner; and (3) dynamically swapping between the normal execution and isolated execution page table maps in response to a change in execution mode, where the change in execution mode involves a context switch. (Ans. 4 .) The Examiner also found that both Coulouris and Silberschatz teach restricting access to an isolated area of memory. (Ans. 5, 24.) The Examiner found that Summers teaches "[r]estricting access to an isolated area of memory to bus cycles performed in the isolated execution mode, . . . where the access to the memory via the bus are [sic] also restricted with a secure bus mechanism." (Ans. 5.) The Examiner determined that it would have been obvious for one of ordinary skill in the art to incorporate Silberschatz's teachings of shared

code processes with Coulouris' teachings of isolated execution processes (Ans. 4, 6) "in order to allow for significant savings in memory while still retaining the logical boundaries of the process to allow for managed concurrent execution." (Ans. 6.) The Examiner also determined that it would have been obvious for one of ordinary skill in the art to incorporate the teachings of Summers' secure bus arbiter (Ans. 5, 6) "to ensure that data may be transferred securely from one module to another within the computer in a way that is compatible with off the shelf, common motherboards." (Ans. 6.)

*Issue 1:* Did Appellants demonstrate that the Examiner erred in establishing a proper prima facie case of obviousness because Coulouris, Silberschatz, and Summers do not teach or suggest restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode?

*Issue 2 – Rejection of Claims 9-15 Under 35 U.S.C. § 103(a) Over Takahashi and Summers*

*Appellants' Contentions*

Appellants contend that the Examiner improperly rejected the claims. Specifically, Appellants contend that the Examiner failed to establish a proper prima facie case of obviousness for the claims in that the Takahashi and Summers references do not teach page table maps, a page table map

selection unit, control registers, or an isolated execution circuit. (App. Br. 8-9.)

*Examiner's Findings and Conclusions*

The Examiner found that Takahashi and Summers teach each feature of Appellants' invention as claimed in independent claims 9 and 12, and dependent claims 10, 11, and 13-15. (Ans. 3-10.) The Examiner found that Takahashi teaches a first storage location storing control data for a first page table map, a second storage location storing control data for a second page table map, and a selection unit. (Ans. 10-11.) The Examiner also found that Takahashi teaches a dual mode processor executing in normal and isolated execution modes, control registers, and a mapping unit. (Ans. 13.) The Examiner found that Summers teaches an isolated execution circuit to generate isolated access bus cycles for use in isolated execution mode. (Ans. 11-12.) The Examiner determined that it would have been obvious for one of ordinary skill in the art to incorporate Summers' teaching of a secure bus arbiter with Takahashi's dual mode processor "to ensure that data may be transferred securely from one module to another within the computer in a way that is compatible with off the shelf, common motherboards." (Ans. 12.)

*Issue 2:* Did Appellants demonstrate that the Examiner erred in establishing a proper prima facie case of obviousness because Takahashi and

Summers do not teach or suggest page table maps, a page table map selection unit, control registers, or an isolated execution circuit?

*Issue 3 – Rejection of Claims 9-15 Under 35 U.S.C. § 103(a) Over Poisner and Summers*

*Appellants' Contentions*

Appellants do not address the Examiner's alternate 35 U.S.C. § 103(a) rejection of claims 9-15 over the Poisner and Summers references.

*Examiner's Findings and Conclusions*

The Examiner found that Poisner and Summers teach each feature of Appellants' invention as claimed in independent claims 9 and 12, and dependent claims 10, 11, and 13-15. (Ans. 17-23.)

*Issue 3:* Did Appellants establish that the Examiner erred in rejecting claims 9-15 as obvious in view of Poisner and Summers?

FINDINGS OF FACT (FF)

We find that the following enumerated findings are relevant to the rejections under review and are supported by at least a preponderance of the evidence. *Ethicon, Inc. v. Quigg*, 849 F.2d 1422, 1427 (Fed. Cir. 1988) (explaining the general evidentiary standard for proceedings before the Office).

*Coulouris Reference*

1. Coulouris describes distributed systems, in particular, distributed operating systems. Coulouris teaches creating processes and execution environments that are by default inaccessible to threads from other processes or execution environments (i.e., secure or isolated). A processor running a secure process operates in isolated execution mode. (Coulouris, 165-66, 168.)

2. Coulouris describes page table maps, and teaches handling different events utilizing page table maps, including events handled by a process operating in isolated execution mode that do not share page tables. Also, Coulouris teaches different page tables access different (i.e., isolated) portions or areas of memory. (Coulouris, 165-169, 190-192.)

3. Coulouris teaches that threads within a process have software interrupts that trigger context switches. Threads may also have handler procedures, and control is transferred to the handler if an interrupt occurs. (Coulouris, 172-173.)

*Silberschatz Reference*

4. Silberschatz describes operating systems. Silberschatz teaches page table maps that are not shared between processes – i.e., utilize their own internal code in an isolated manner (isolated execution mode) – and page table maps that are shared between processes – i.e., normal execution mode. (Silberschatz, 270-272.)

5. Silberschatz teaches switching between processes in response to interrupts. (Silberschatz, 92.)

*Appellants' Admitted Prior Art*

6. Appellants concede that the Coulouris and Silberschatz references teach: "A process executing in a virtual memory system has a page table. Some page tables may be exclusive to one process, while other page tables may contain entries shared between two or more processes. An operating system ("OS") may perform a context switch from one process to another in response to a software or hardware interrupt." (App. Br. 5.)

*Summers Reference*

7. Summers describes computer data bus controllers, in particular, a secure bus arbiter (SBA) and controller. The SBA controls access to data buses among different system elements (e.g., memory), establishing an isolated bus for transmitting a particular class of data, and preventing unauthorized devices from accessing or affecting the particular data. (Summers, Abstract; col. 1, ll. 15-26; col. 2, l. 37 to col. 3, l. 62; col. 5, ll. 29-33; col. 6, ll. 1-7.)

8. Summers' SBA is responsive to a trusted system element, and operates in any standard system architecture with any commercial off the shelf motherboard. (Col. 1, ll. 48-54; col. 4, ll. 15-26, 45-51; col. 6, ll. 24-61.)

*Takahashi Reference*

9. Takahashi describes a dual mode processor operating in a secure (isolated) mode. (Col. 1, ll. 36-54; col. 2, ll. 47-48; col. 3, ll. 48-59.)

10. Takahashi's processor may operate in either normal mode or secure mode. In the normal mode, the processor receives external instructions and accesses its random access memory (RAM). In the secure mode, the processor only executes secure primitives (instructions) stored in its read only memory (ROM). (Col. 2, ll. 47-60; col. 3, ll. 26-59; col. 4, ll. 15-57.)

11. Takahashi's processor enters the secure mode in response to a special interrupt. The interrupt includes a memory address for a secure function in the ROM. A secure mode entry routine in the ROM uses internal pointers to access the secure functions stored in the ROM. (Col. 3, ll. 26-59; col. 4, ll. 15-57; Figs. 4-5.)

12. Takahashi describes mapping the memory location of a secure function located (stored) in the processor ROM. (Col. 1, ll. 41-50; col. 4, ll. 31-35, 48-51; Figs. 4-5.)

PRINCIPLES OF LAW

*Burden on Appeal*

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

*Obviousness*

A claimed invention is not patentable if the subject matter of the claimed invention would have been obvious to a person having ordinary skill in the art. 35 U.S.C. § 103(a); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007); *Graham v. John Deere Co.*, 383 U.S. 1, 3 (1966).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," and stated that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 550 U.S. at 415-16. The Court explained:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

*Id.* at 417. The operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.*

Consistent with *KSR*, the Federal Circuit recently recognized that "[a]n obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some

combinations would have been obvious where others would not." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR,* 550 at 416). The Federal Circuit relied in part on the fact that *Leapfrog* had presented no evidence that the inclusion of a reader in the combined device was "uniquely challenging or difficult for one of ordinary skill in the art" or "represented an unobvious step over the prior art." *Id.* at 1162.

## ANALYSIS

*Rejection of claims 1-8 Under 35 U.S.C. § 103(a)*

Initially we note the following claim grouping. Appellants argue the merits of only independent claim 1. They do not address dependent claims 2-8. (App. Br. 3, 5-8.) We will, therefore, treat claims 2-8 as standing or falling with claim 1. We accept Appellants' grouping of the claims. *See* 37 C.F.R. § 41.37(c)(1)(vii) ("Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately."). Accordingly, we address only those arguments that Appellants present in the Brief. Arguments that Appellants could have made but chose not to make in the Brief are waived.

*Issue 1 – Do the References Teach Restricting Access To An Isolated Area Of Memory To Bus Cycles Performed In The Isolated Execution Mode?*

The Examiner rejects claim 1 under 35 U.S.C. § 103(a) over Coulouris, Silberschatz, and Summers. Appellants contend that the references do not teach the invention claimed in claim 1 – specifically, restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode – and are not properly combinable. (App. Br. 5-7.) The Examiner found that the references teach each limitation of claim 1, including restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode. (Ans. 3-5, 23-27.) The Examiner also determined that references are properly combinable, and that one of skill in the art would have been motivated to combine the references. (Ans. 4, 5, 6, 28.) We decide the question of whether Appellants demonstrate that the Examiner erred in establishing a proper prima facie case of obviousness because the references (Coulouris, Silberschatz, and Summers) do not teach or suggest restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode. We also decide whether the references are properly combinable. We will affirm the Examiner's rejection of claim 1, and 2-8 for the reasons that follow.

Coulouris and Silberschatz both describe operating systems, and teach the interaction of virtual memory mapping, process generation, process execution, threads, interrupts, and context switches. (FF 1-6; Ans. 3-5, 23-27.) Coulouris and Silberschatz teach each feature of claim 1, except

restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode. These features include: (1) maintaining a first page table map for use in an isolated execution mode and a second page table map for use in a normal execution mode (FF 1, 2, 4, 6; Ans. 4); (2) dynamically swapping between the first page table map and the second page table map responsive to a change in execution mode (FF 5, 6; Ans. 4); (3) identifying if an event is one of a class of events to be handled in the isolated execution mode (FF 1-3, 6; Ans. 3); asserting a selection signal to select the first page table map if the event is identified as one of the class of events to be handled in the isolated execution mode (FF 1-3, 6; Ans. 3); and handling the event using a table map selected by the selection signal (FF 1-3, 6; Ans. 3).

Coulouris, Silberschatz, and Summers together teach the remaining claimed feature – restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode. Coulouris and Silberschatz teach isolated execution mode processes, and restricting access by processes and/or threads to isolated portions of memory. (FF 1, 2, 4; Ans. 5, 24, 25.) Summers teaches a secure bus arbiter (SBA) responsive to a trusted system element establishing an isolated bus for transmitting a particular class of data between system elements and memory. The SBA prevents unauthorized devices from accessing or affecting the data in memory, and operates in any standard system architecture with any commercial off the shelf motherboard. (FF 7-8.) Summers, therefore,

teaches restricting access to memory by isolating bus access to only authorized devices, i.e., to memory access transactions (bus cycles) from authorized devices. Accordingly, we find the combination of references teaches restricting access to isolated portions (area) of memory to bus cycles (transactions) from authorized devices in isolated execution mode.

Contrary to Appellants' assertions, we find that Summers is not incompatible with Coulouris and Silberschatz, or with the claimed invention. Summers specifically teaches that the SBA can establish separate buses for each class of data between elements of a computer system as needed. (Col. 2, ll. 55-60.) Memory is a computer system element. Summers also specifically teaches that the SBA is compatible with all known buses and most architectures – "All known standard computer buses have data lines that can be readily blocked with bus transceivers," [a]ll computer buses employ bus arbitration schemes that can be readily intercepted and overlaid with data class-system element associations," and "the SBA applies to virtually any standard bus" permitting "the SBA of the present invention to provide data security in a wide variety of commercial architectures." (Col. 3, ll. 52-62.) The SBA "accomplishes this process in the same time that the normal hardware bus arbitration would require," thus, "bus performance is not impacted." (Col. 3, ll. 42-46.) Accordingly, limiting access to a bus, as taught by Summers, would actually enhance the memory access limiting functionality taught by Coulouris and Silberschatz. Such an enhancement is tantamount to the predictable use of prior art elements according to their

established functions – an obvious improvement. *KSR*, 550 U.S. at 417. We also note that the Examiner provides ample evidence of reasons to combine the references. (Ans. 4, 5, 6, 28.) Thus, we are not persuaded by Appellants' arguments against the combinability of Coulouris, Silberschatz, and Summers. In light of *KSR* and *Leapfrog*, the evidence provided by the Examiner supports a finding that combining familiar elements according to known methods is obvious when it does no more than yield predictable results.

For all the reasons noted above, Appellants fail to demonstrate error in the Examiner's rejection of claim 1 and claims 2-8. Accordingly, we will sustain the Examiner's rejection of claims 1-8.

*Rejection of claims 9-15 Under 35 U.S.C. § 103(a)*

Initially we note that Appellants argue the merits of only independent claims 9 and 12. They do not address dependent claims 10 and 11, or 13-15. (App. Br. 3, 8-9.) We will, therefore, treat claims 10 and 11 as standing or falling with claim 9, and claims 13-15 as standing or falling with claim 12. *See* 37 C.F.R. § 41.37(c)(1)(vii).

*Issue 2 – Do the References Teach Page Table Maps, a Page Table Map Selection Unit, Control Registers, and an Isolated Execution Circuit?*

The Examiner rejects claims 9 and 12 under 35 U.S.C. § 103(a) over Takahashi and Summers. Appellants contend that the references do not

teach the invention claimed in claim 9 – specifically, a page table map, a selection unit, and an isolated execution circuit. (App. Br. 8.) Appellants also contend that the references do not teach the invention claimed in claim 12 – specifically, control registers, a memory map, and an isolated execution circuit. (App. Br. 9.) The Examiner found that the references teach each limitation of claims 9 and 12, including a page table map (memory map), control registers, a selection unit, and an isolated execution circuit. (Ans. 11-12, 13-14, 29-31.) The Examiner also determined that one of skill in the art would have been motivated to combine the references. (Ans. 12, 14.) We decide the question of whether Appellants demonstrate that the Examiner erred in establishing a proper prima facie case of obviousness because Takahashi and Summers do not teach or suggest a page table map, control registers, a selection unit, and an isolated execution circuit. We will affirm the Examiner's rejection of claims 9 and 12, and claims 10, 11, and 13-15 for the reasons that follow.

We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims "their broadest reasonable interpretation consistent with the specification" and "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted).

Accordingly, giving the "control data for a [ ] page table map" and "control register" limitations their broadest reasonable interpretation, we

find that a control data for a page table map and control registers are data for a memory map that maps virtual memory address to physical memory addresses (*see* Ans. 24-25).

Although not explicitly described, Takahashi suggests using memory maps to access instructions or data, i.e., memory mapping. Takahashi teaches accessing instructions or data in a processor RAM (first memory location). (FF 10.) In a virtual memory system, in order to access instructions, a memory map is necessary. This memory map must include data (control registers) relating the virtual and physical memory addresses. Thus, as found by the Examiner, Takahashi teaches control data for page table maps and control registers. (Ans. 11, 13, 29.) We also find that Takahashi teaches control data for first page table map (memory map) stored in a first storage location, as well as a first set of control registers to define a current (first location) memory map.

Takahashi expressly describes a processor ROM, an isolated (secure) execution mode, and accessing functions in the processor ROM in isolated execution mode. (FF 9-12.) Accordingly, Takahasi teaches control data for a second page table map (memory map) in a second storage location, as well as, a mapping unit to dynamically load control registers using an alternate memory map.

As previously explained (*supra*), Summers teaches an isolated execution circuit to generate isolated access bus cycles to be used in isolated execution mode.

We also note that the Examiner provides ample evidence of reasons to combine the references. (Ans. 12, 14.) Thus, in light of *KSR* and *Leapfrog*, the evidence provided by the Examiner supports a finding that combining familiar elements according to known methods is obvious when it does no more than yield predictable results.

For all the reasons noted above, Appellants fail to demonstrate error in the Examiner's rejection of claims 9-15. Accordingly, we will sustain the Examiner's rejection of claims 9-15.

*Issue 3 – Do Appellants Establish that the Examiner erred in rejecting claims 9-15 as obvious in view of Poisner and Summers?*

The Examiner found that Poisner and Summers teach each feature of Appellants' invention as claimed in independent claims 9 and 12, and dependent claims 10, 11, and 13-15. (Ans. 17-23.) As we noted previously, *supra*, Appellants do not address the Examiner's alternate 35 U.S.C. § 103(a) rejection of claims 9-15 over the Poisner and Summers references. Accordingly, Appellants waive any arguments of the patentability of claims 9-15 over Poisner and Summers. *See* 37 C.F.R. § 41.37(c)(1)(vii).

CONCLUSION OF LAW

On the record before us, we find that Appellants do not demonstrate that the Examiner erred in establishing a proper prima facie obviousness rejection for: (1) claims 1-8, in that Coulouris, Silberschatz, and Summers teach restricting access to an isolated area of memory to bus cycles

performed in the isolated execution mode; (2) claims 9-15, in that Takahashi and Summers teach page table maps, a page table map selection unit, control registers, and an isolated execution circuit; and (3) claims 9-15 over Poisner and Summers, in that Appellants failed to address the rejection.

## DECISION

We affirm the Examiner's rejection of claims 1-15 under § 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rwk

Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025